15.5 Analog Signal Processing with Organic FETs

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The advent of organic field-effect transistors for low-performance applications requires the design of analog circuits capable of handling the most basic analog signal processing [1,5]. However, successful design relies heavily on the quality of the underlying OFET model and this in turn on the available technological process.

Bottom-gate coplanar transistors (Fig. 15.5.1) are built using a four-layer process: Ti gates are deposited on a glass or thermally oxidized Si substrate, followed by a 100nm thick polyvinylphenol (PVP) insulator layer and Au S/D contacts, all patterned by photolithography and etching. Circuits are completed by evaporating a 30nm thick pentacene layer through a stencil mask. The technology presented is composed only of p-type transistors and capacitors.

The model [1,2] is directly derived from the measured OFET characteristics. It is subdivided into: (i) a physical submodel, where all relevant design parameters are involved (geometry), and (ii) a numerical submodel, which contains a detailed description of the transistor behavior. A reference transistor is used upon which measurements are extracted, accordingly defining a reference set of characteristics. The transistor channel current is described by a single equation (1), thus improving simulation speed and stability. Four factors can be identified in the equation:

$$I_{ds} = K_G \cdot f\left(\frac{U_{ds}}{\tau(U_{gs})}\right) \cdot h(U_{gs}) \tag{1}$$

1 - The geometry factor K_G Eqn. (2) includes geometry and technological constants. It is normalized to the geometry constants of the reference transistor;

$$K_G = \frac{\frac{W}{L} \cdot \frac{\varepsilon_r \cdot \varepsilon_0}{d_{ox}}}{\left[\frac{W}{L} \cdot \frac{\varepsilon_r \cdot \varepsilon_0}{d_{ox}}\right]_R} = \frac{W/L}{W_R/L_R} \tag{2}$$

2 - The shape function f Eqn. (3) establishes the direction and magnitude of the current, reproducing a typical current characteristic, i.e. the characteristic for fixed U_{gs} and a particular W/L ratio. This factor can be regarded as a shape function, since the mapped curve will be scaled, stretched and shifted by other terms in the final equation;

$$f(U_{ds}) = -10^X$$
$$X = \sum_i a_i \cdot \exp(-b_i \cdot U_{ds}) \tag{3}$$

3 - The scale function $h(U_{gs})$ Eqn. (4) *vertically* scales f partly reproducing the transfer characteristic;

$$h(U_{gs}) = 10^X$$
$$X = \sum_i c_i \cdot \exp(-d_i \cdot U_{gs}) \tag{4}$$

4 - The delay function $\tau(U_{gs})$ Eqn. (5) *horizontally* stretches the shape function f.

$$\tau(U_{gs}) = 10^X$$
$$X = \sum_i p_i \cdot \exp(-q_i \cdot U_{gs}) \tag{5}$$

Using this mathematical model, it is possible to fit measurement data precisely (Fig. 15.5.1). The parameters of f are easily determined for a particular gate bias U_{gs0}, where the condition $\tau(U_{gs0}) = h(U_{gs0}) = 1$ is imposed, then we have $I_{ds} = f(U_{ds})$ since $K_G = 1$ for the reference transistor. With this condition, f can be fitted to the measured current values I_{ds}. The parameters of h and τ are determined simultaneously using a multivariate optimization algorithm. The dynamic FET model also considers hysteresis effects [2,4,5]. An RC-network is added to simulate the delayed transport of mobile charges in the insulator [4]. The statistical transistor model Eqn. (6) introduces three stochastic variables: the current scale factor K_s, the switch-on voltage shift U_{on} and the saturation regime delay shift τ_s. All of them are modeled with normal density functions whose parameters were extracted from measurements. Parameter values are summarized in Fig. 15.5.2.

$$I_{ds} = K_S \cdot K_G \cdot f\left(\frac{U_{ds}}{\tau + \tau_s}\right) \cdot h(U_{gs} - U_{on}) \tag{6}$$

A partial view of the test chip is seen in Fig. 15.5.3. Most bias voltages are generated internally by means of voltage dividers. Also included are output stages to handle the capacitive load of the probe needles. All measurements are contrasted against Monte-Carlo (MC) simulations. The statistical OFET parameters are assumed to be uncorrelated. Based on a number of MC runs, a normalized probability density function (PDF) can be estimated for each time or frequency point. With it, a particular confidence level and a most probable region can be determined. Three test circuits, described below, have been characterized.

In the cascode common-source amplifier the common-gate connected transistor M2 buffers M1 (Fig. 15.5.4), thereby increasing the output impedance, which leads to a gain boost over a regular common-source amplifier. C_{gd1} is reduced but no bandwidth improvement is attained, since C_{gs1} is the dominant parasitic (hysteresis). A unity bandwidth of 1.4kHz is measured (Fig. 15.5.5).

Input and output signals in a Differential Amplifier (DA) should have an offset of zero. However, practical circuits have an offset due to degradations in transistor matching, i.e. asymmetries in the circuit branches M1-M3 and M2-M4 (Fig. 15.5.6). The CMMR of the circuit is degraded because of the finite output impedance of M5. Moreover, AC-signals are leaked through the parasitic capacitance at the current summing node, further reducing the output impedance of M5 at higher frequencies. Nonetheless, the differential gain of the circuit has a frequency response equivalent to that of a regular common-source amplifier.

The Differential-to-single-ended converter (DSEC) of Fig. 15.5.7 is made up of transistors M6-M9. The kernel of the practical circuit is a DA (M1-M5). The differential outputs are fed into the gates of M6 and M7, working as source followers. M8 is the load of M6 and serves also to inject the signal at the gate of M9. The latter is seen by the signal at its gate as a common-source connected transistor. Assuming that the source followers M6-M8 and M7-M9 have a gain of 1, the common-source amplifier M9-M7 should have a gain of -1 in order to add the differential outputs at the output node in phase. Due to the non-ideal transfer of the source followers, the DC-gain is considerably degraded. Simulation predicts a gain reduction of 6dB below that of the differential amplifier (~10dB), so that the overall gain of the circuit should be app. 4dB, which agrees with our measurements (4.3dB).

Though the performance of these devices falls behind their silicon counterparts, they are nonetheless suitable for interfacing simple sensors, where requirements, i.e. the response speed, are not critical. To account for variations in the transistor parameters, the design of circuits heavily relies upon statistical analysis. Future investigations will concentrate on using switched capacitor techniques to eliminate, much of the uncertainty in the transistor characteristics.

References:

[1] Gay N., *Analog Circuits based on Polymer Field-effect Transistors*, PhD Thesis. Dresden University of Technology, 2005 (TBP).
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[3] Gregorian R., Analog MOS Integrated Circuits for Signal Processing. Wiley, New York, 1986.
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[5] Kane M.G. et al., *Analog and Digital Circuits Using Organic Thin-Film Transistors on Polyester Substrates*, *IEEE El. Dev. Lett.*, vol. 21 no. 11, pp. 534, Nov., 2000.

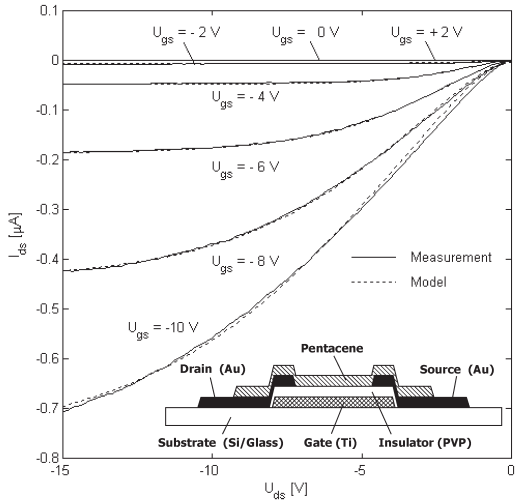

Figure 15.5.1: OFET output characteristic and transistor cross-section.

Key Technological Transistor Parameters			
Width (*W*)	5…300 µm	Switch-on Volt.	5…8 V
Length (*L*)	5…50 µm	Subthr. Swing	3…5 V/dec
Diel. Thickness	100 nm	Mobility	0.1…0.3 cm^2/Vs
Rel. Permittivity	3.6	C_{ox}'	0.32 fF/µm^2
Static Transistor Model			
Shape function *f*			
a_1	-1.2737	b_1	0.4115
a_2	-6.7432	b_2	1.20e-4
a_3	-1.0077	b_3	1.9633
Scale function *h*		Delay function τ	
c_1	-3.8416	p_1	-1.9399
c_2	0.8047	p_2	1.1035
d_1	0.2432	q_1	0.1215
d_2	-0.0175	q_2	0.0277
Dynamic Transistor Model			
Capacitance Model		Statistical Model – Range (Av.)	
U_c [V]	1.5	τ_s	-1…1 (0)
U_{ds0} [V]	-6	K_s	0…2 (1)
		U_{on} [V]	-5…5 (0)
Typical Small-Signal Parameter Values			
Parameter	Range (Av.)	Comment	
g_m [nA/V]	140…<1 (41)	Ref. OFET *W* = 50µm, *L* = 5µm	
g_{ds} [nS]	100…<1 (27)	U_{gs0} = -15…0V, U_{ds0} = -15…0V	
C_{as} [fF/µm]	1.7…1.4 (1.56)	L_{ov} = 2µm	
C_{gd} [fF/µm]	1.4…0.6 (1.04)	U_{gs0} = -15…0V, U_{ds0} = -15…0V	
C_{hys} [fF/µm^2]	4	Estimated. C_{hys}^{ref} = 1pF	
R_{hys} [Ω]	1e5	(*W*.*L* = 250µm^2)	

Figure 15.5.2: Transistor and model parameters.

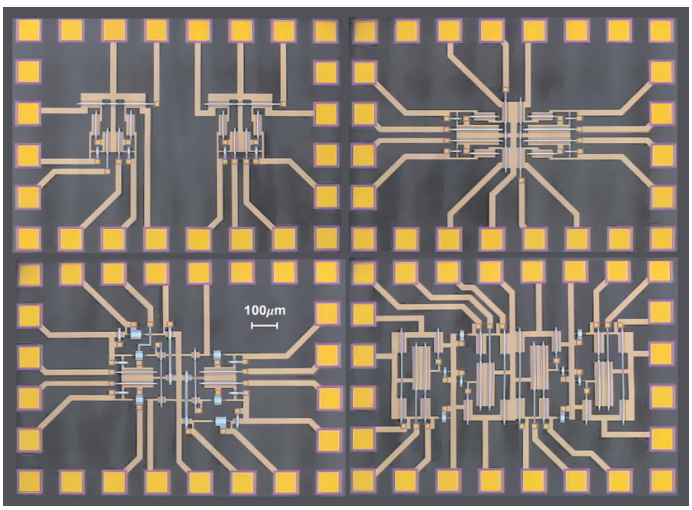

Figure 15.5.3: Die Photo.

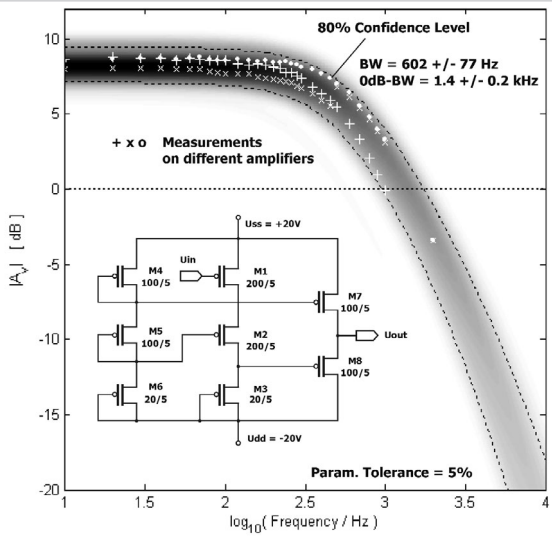

Figure 15.5.4: Frequency response and circuit schematic of the cascode amplifier.

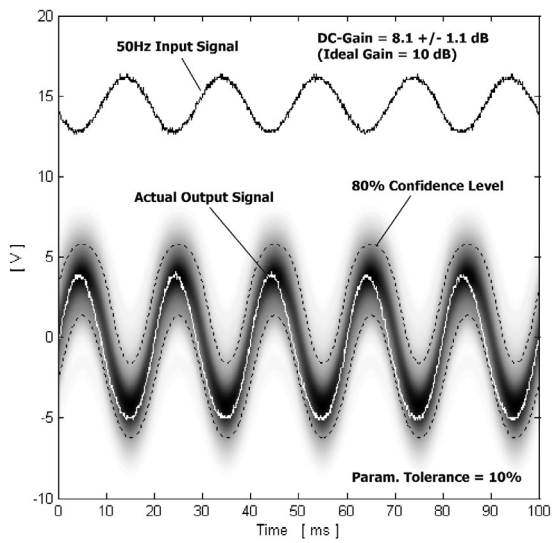

Figure 15.5.5: Time response of the cascode amplifier.

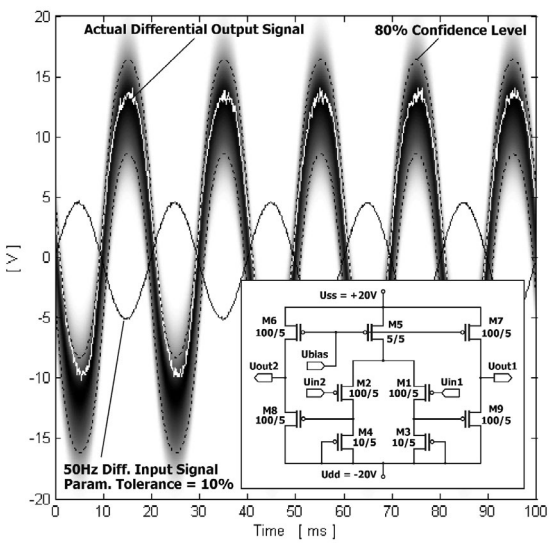

Figure 15.5.6: Time response and circuit schematic of a differential amplifier.

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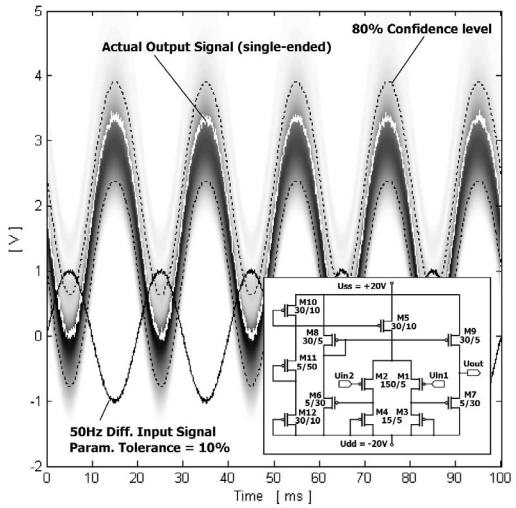

Figure 15.5.7: Time response and circuit schematic of a diff.-to-single-ended converter.

